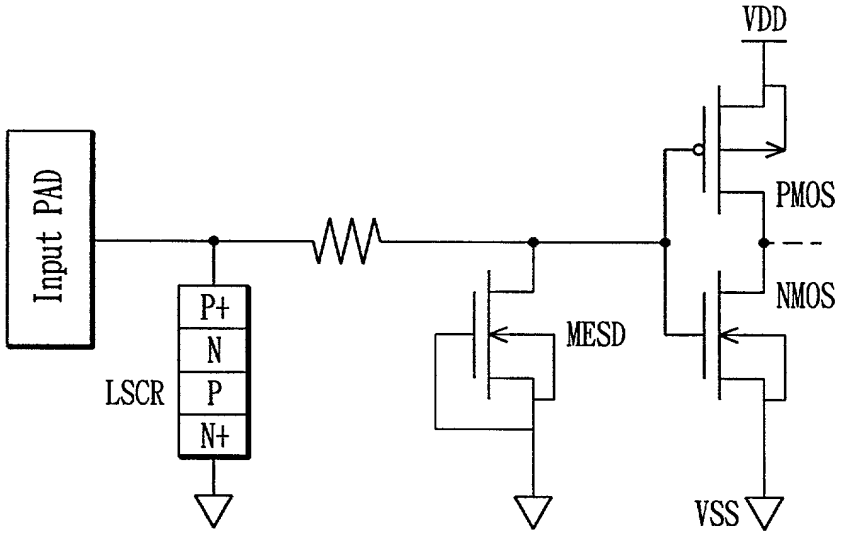

FIG. 1a (PRIOR ART)

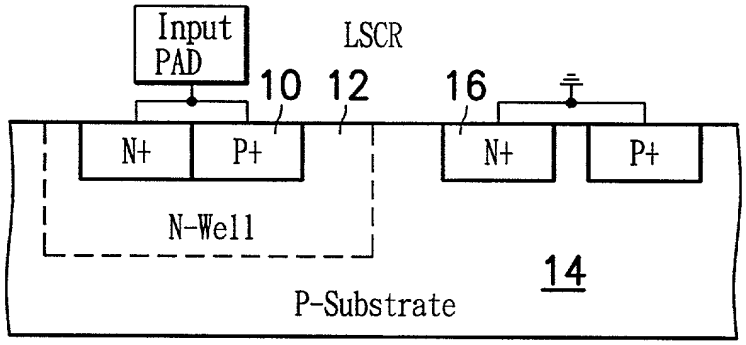

FIG. 1b (PRIOR ART)

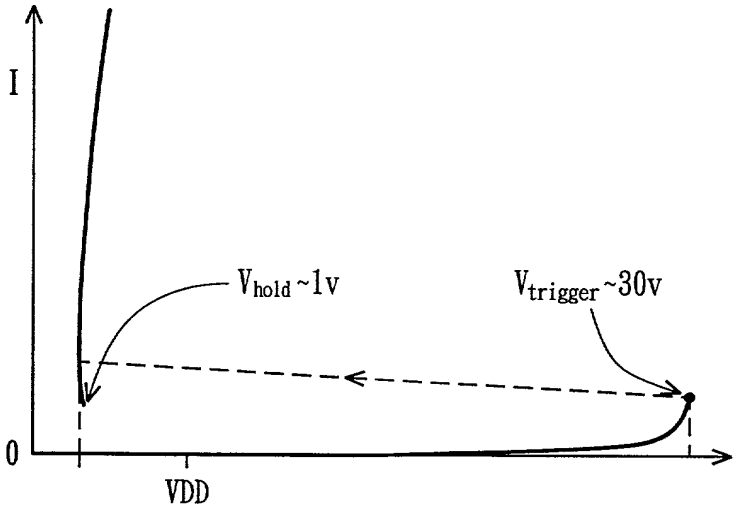

FIG. 1c (PRIOR ART)

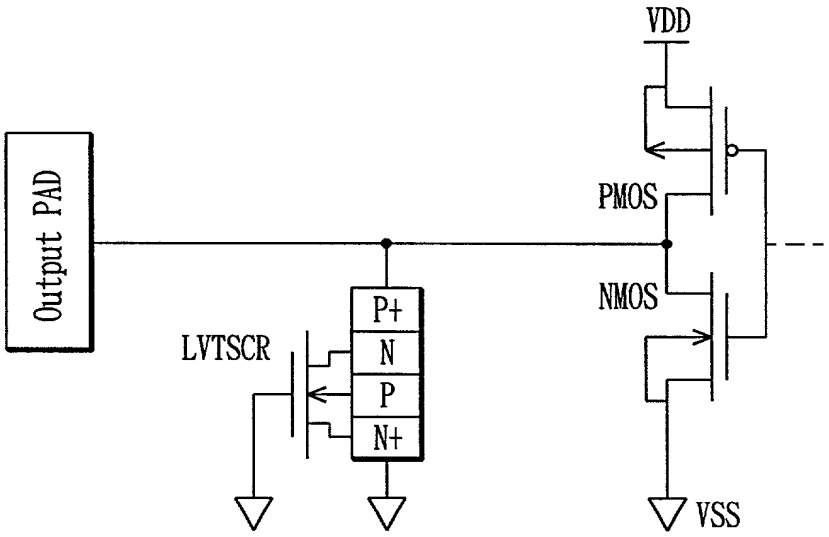

FIG. 2a (PRIOR ART)

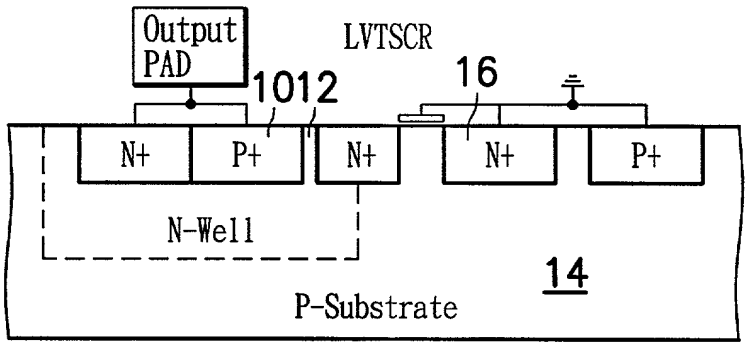

FIG. 2b (PRIOR ART)

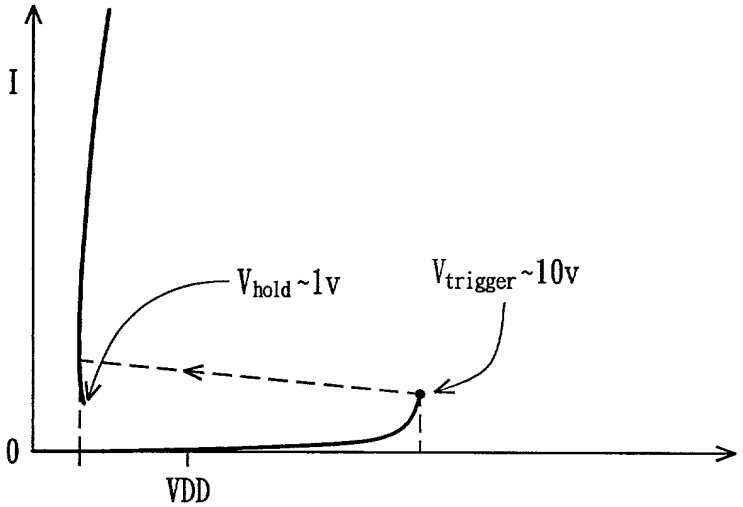

FIG. 2c (PRIOR ART)

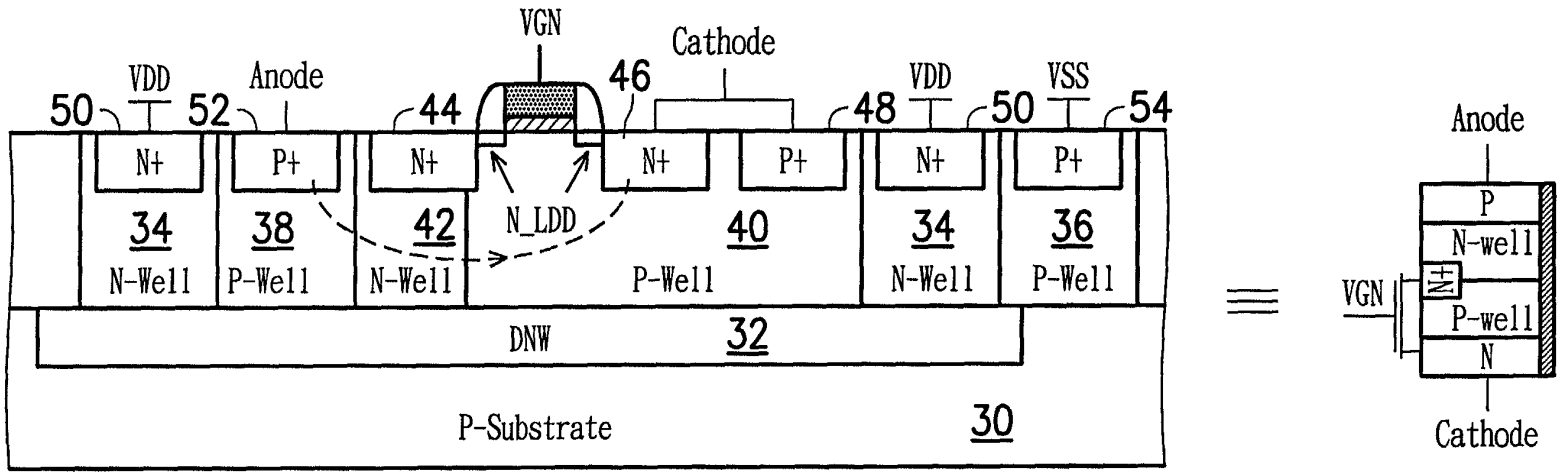

FIG. 3a

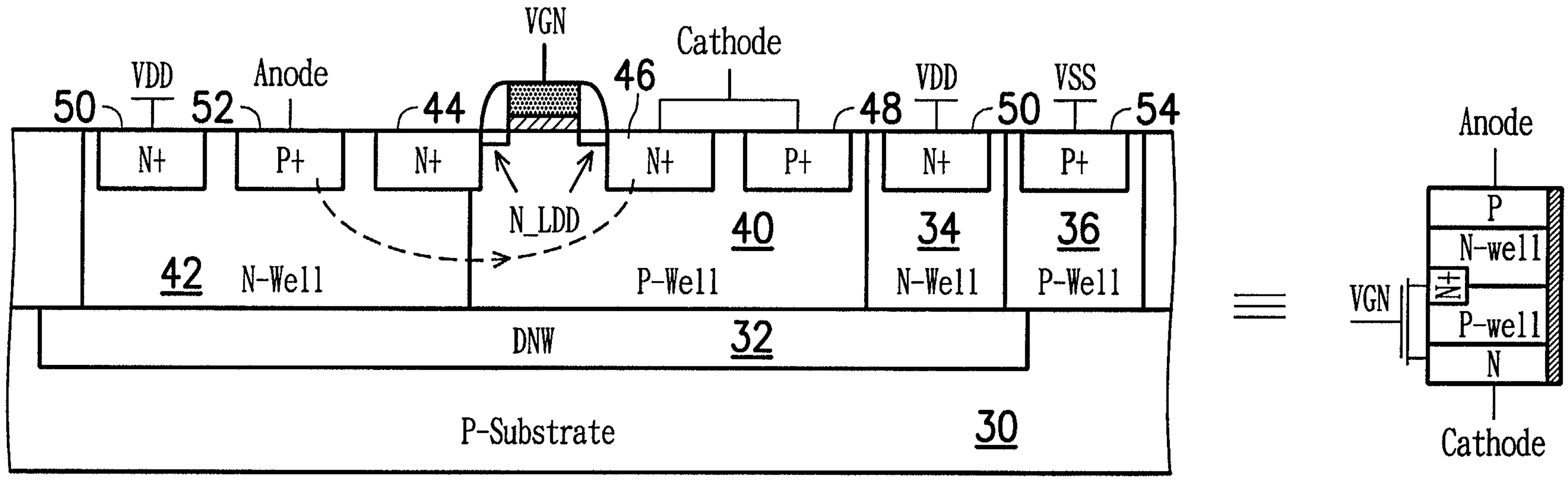

FIG. 3b

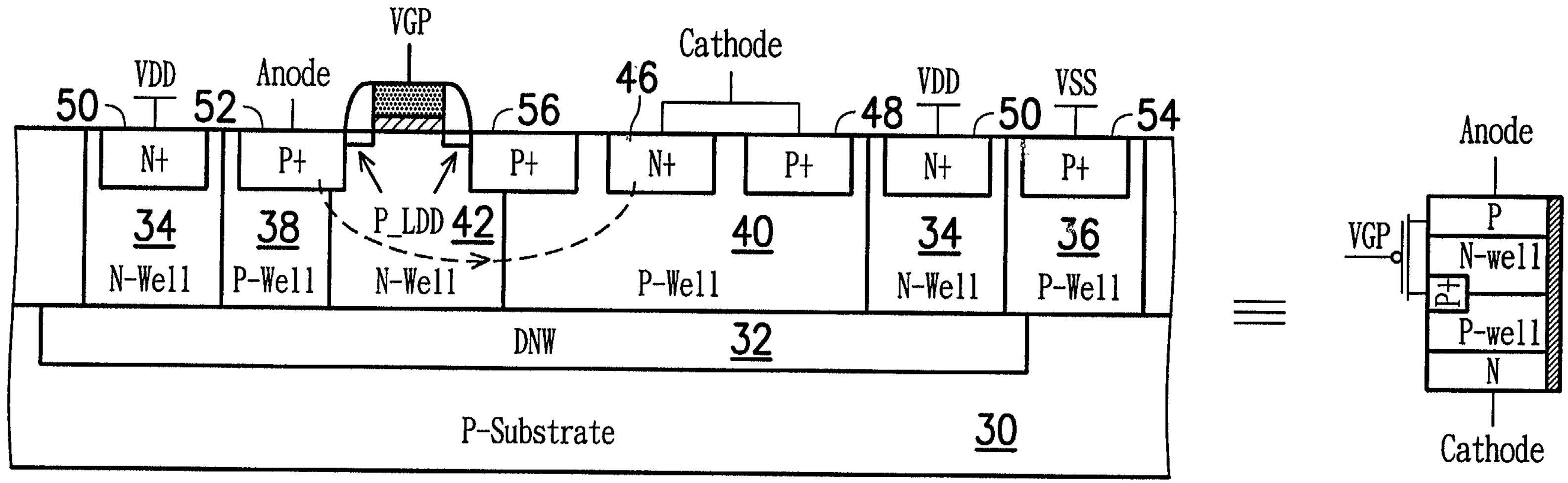
VGP
Cathode
50
VDD
52
Anode
56
46
48
VDD
50
VSS
54
N+
P+
P+
N+
P+
N+
P+
34
N-Well
38
P-Well
P_LDD 42
N-Well
40
P-Well
34
N-Well
36
P-Well
DNW
32
P-Substrate
30
Anode
VGP
P
N-well
P+
P-well
N
Cathode

FIG. 4a

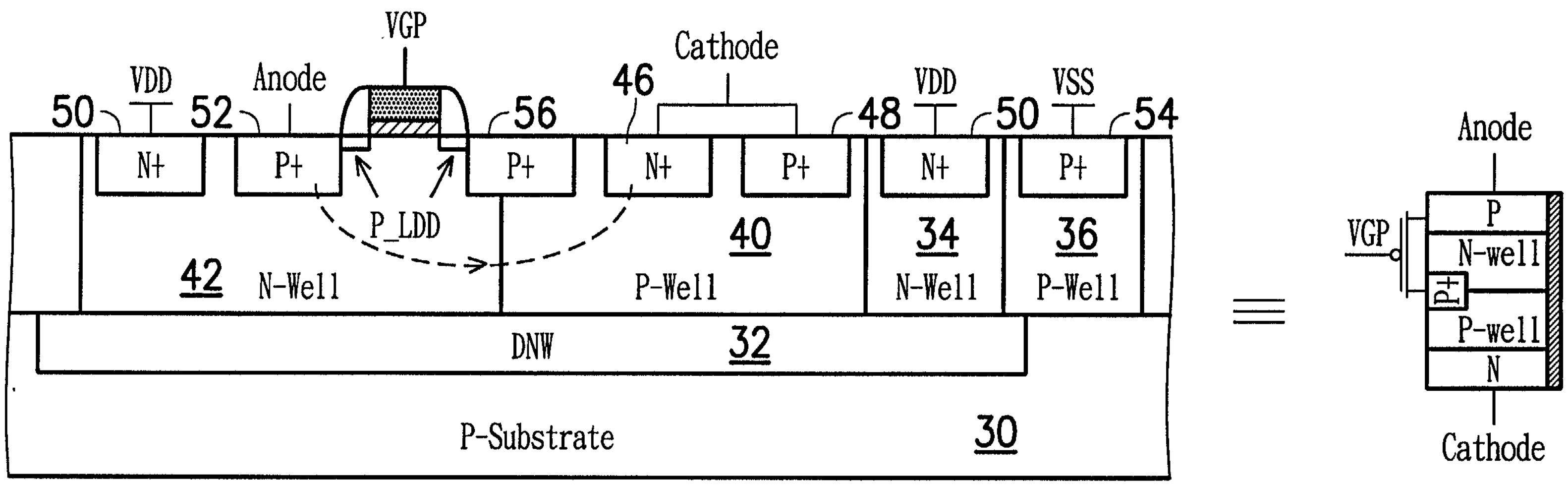

FIG. 4b

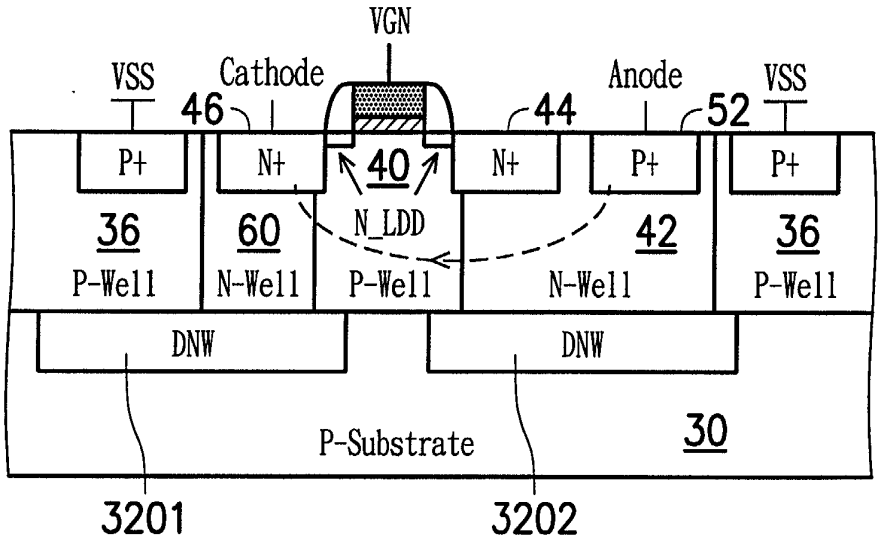
VGN
VSS
Cathode
Anode
VSS
46
44
52
P+
N+
40
N+
P+
P+
36
60
N_LDD
42
36
P-Well
N-Well
P-Well
N-Well
P-Well
DNW
DNW
P-Substrate
30
3201
3202

FIG. 5

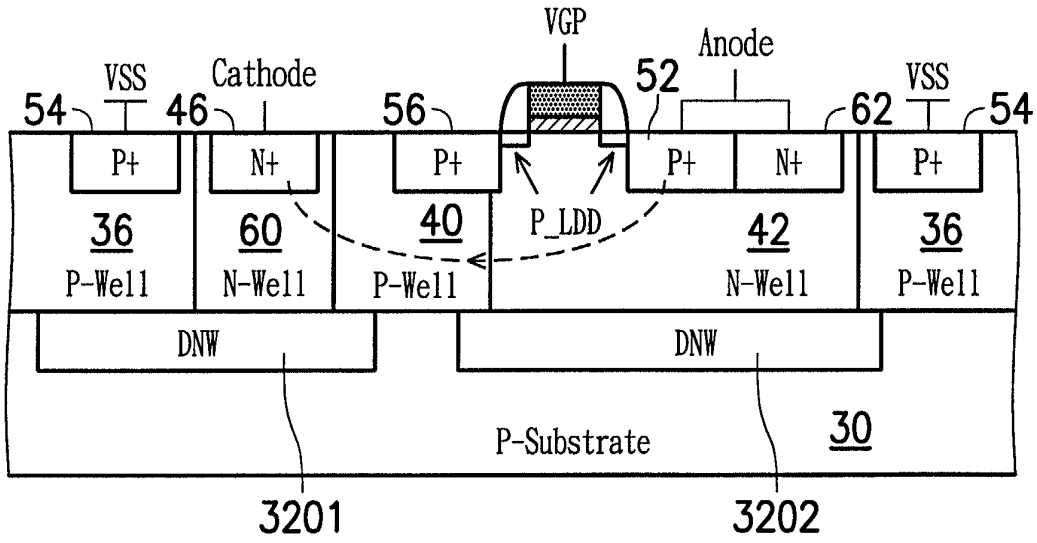
VGP
Anode
VSS
Cathode
VSS
54
46
56
52
62
54
P+
N+
P+
P+
N+
P+
36
60
40
P_LDD
42
36
P-Well
N-Well
P-Well
N-Well
P-Well
DNW
DNW
P-Substrate
30
3201
3202

FIG. 6

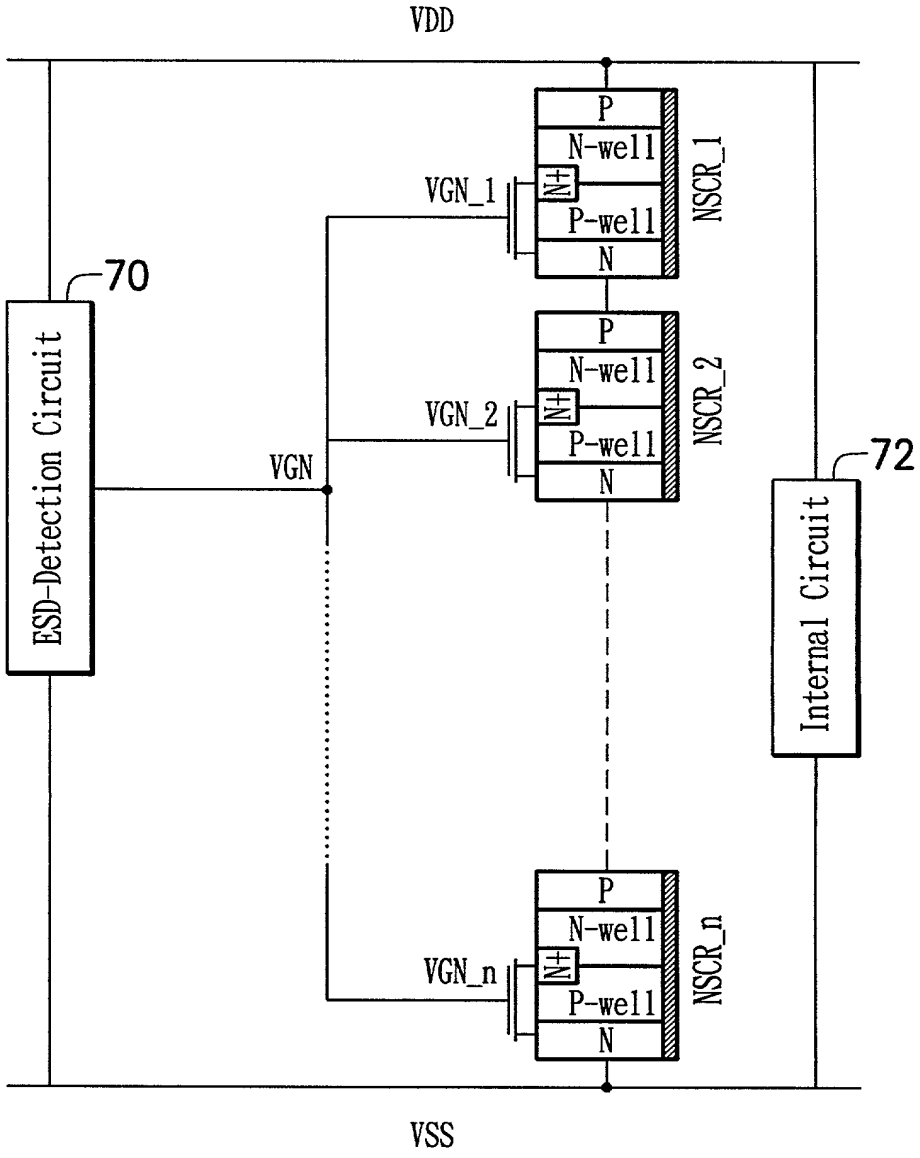
VDD
P
N-well
N+
P-well
N
NSCR_1
VGN_1
NSCR_2
VGN_2
NSCR_n
VGN_n
VGN
70
ESD-Detection Circuit
72
Internal Circuit
VSS

FIG. 7

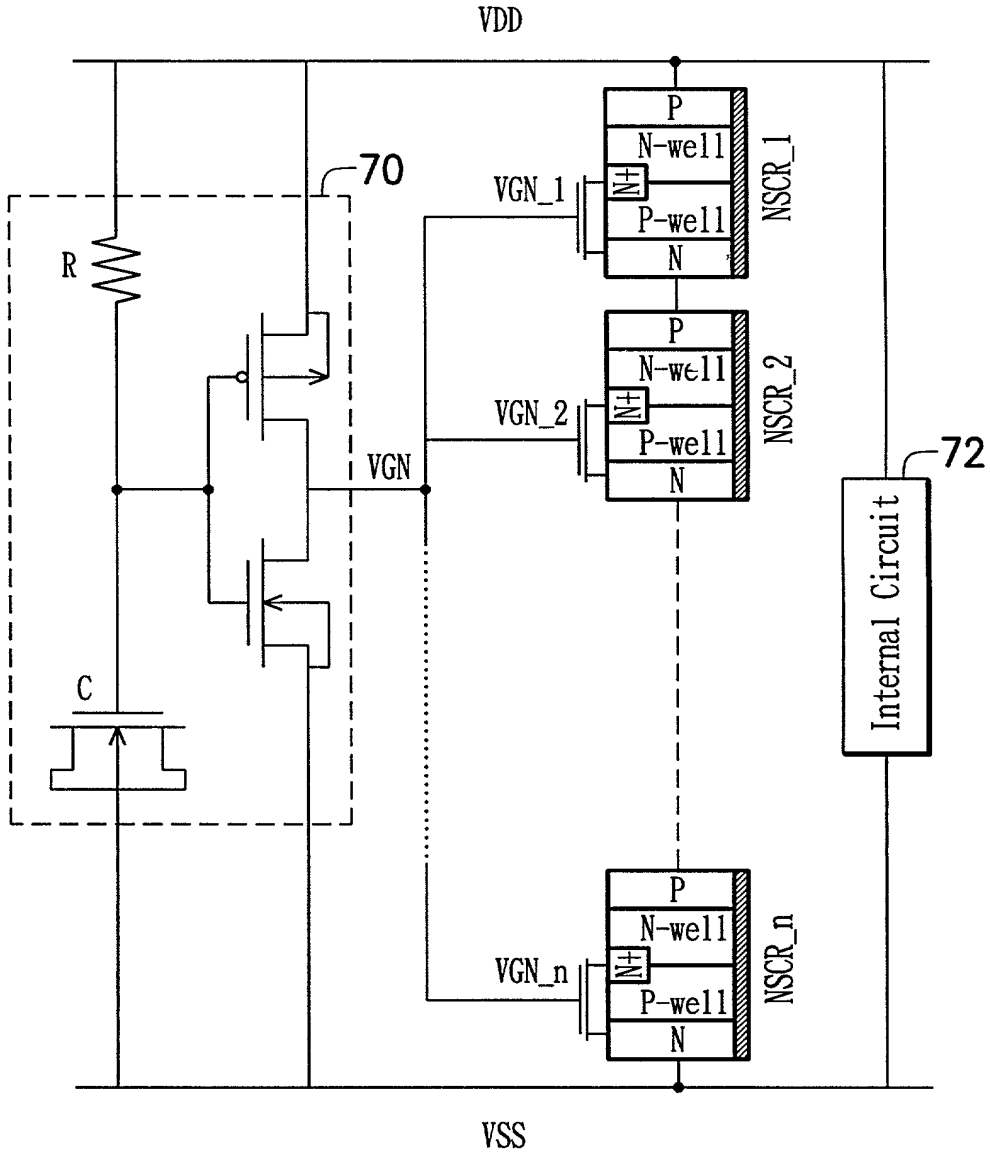
VDD
70
R
C
VGN
VGN_1
VGN_2
VGN_n
P
N-well
N+
P-well
N
NSCR_1
NSCR_2
NSCR_n
72
Internal Circuit
VSS

FIG. 8

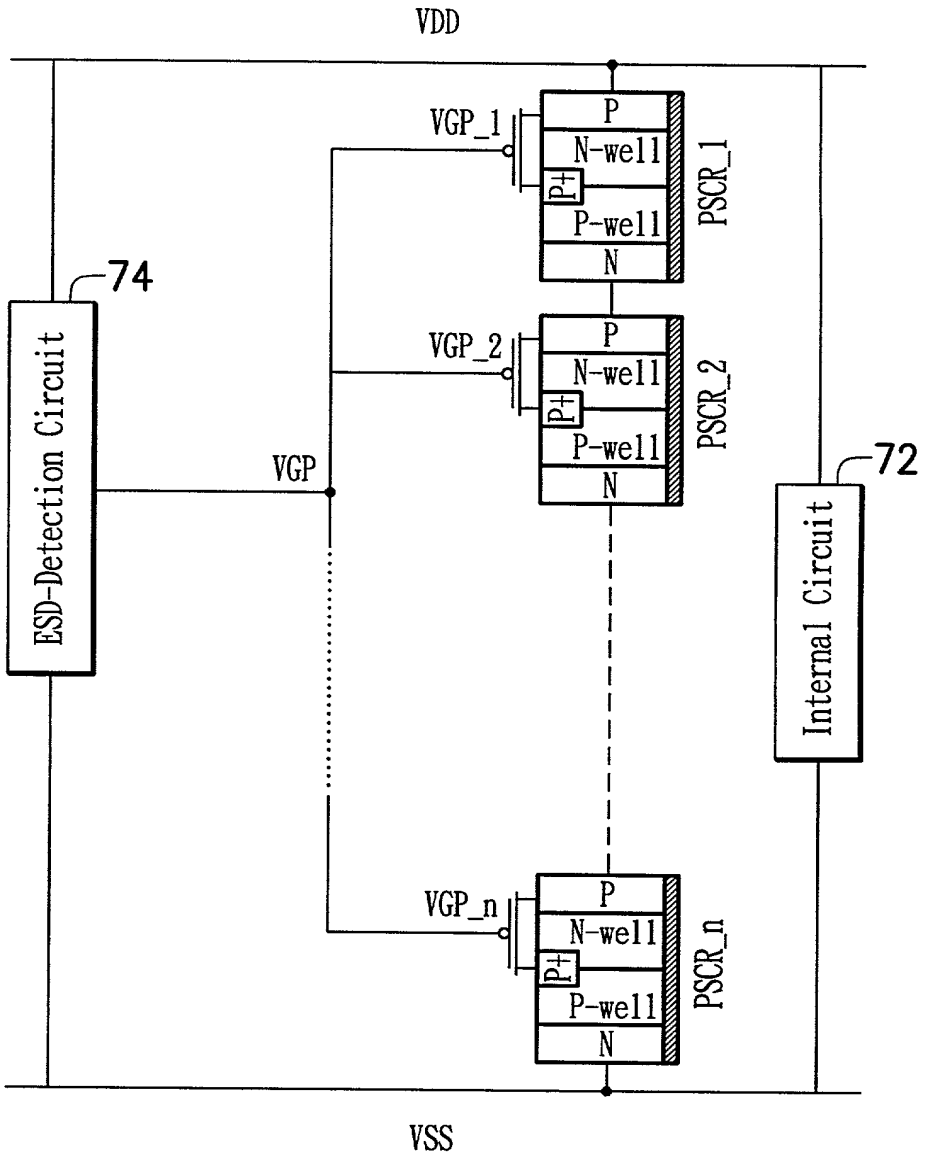
VDD
VGP_1
P
N-well
P+
P-well
N
PSCR_1
74
VGP_2
P
N-well
P+
P-well
N
PSCR_2
VGP
72
ESD-Detection Circuit
Internal Circuit
VGP_n
P
N-well
P+
P-well
N
PSCR_n
VSS

FIG. 9

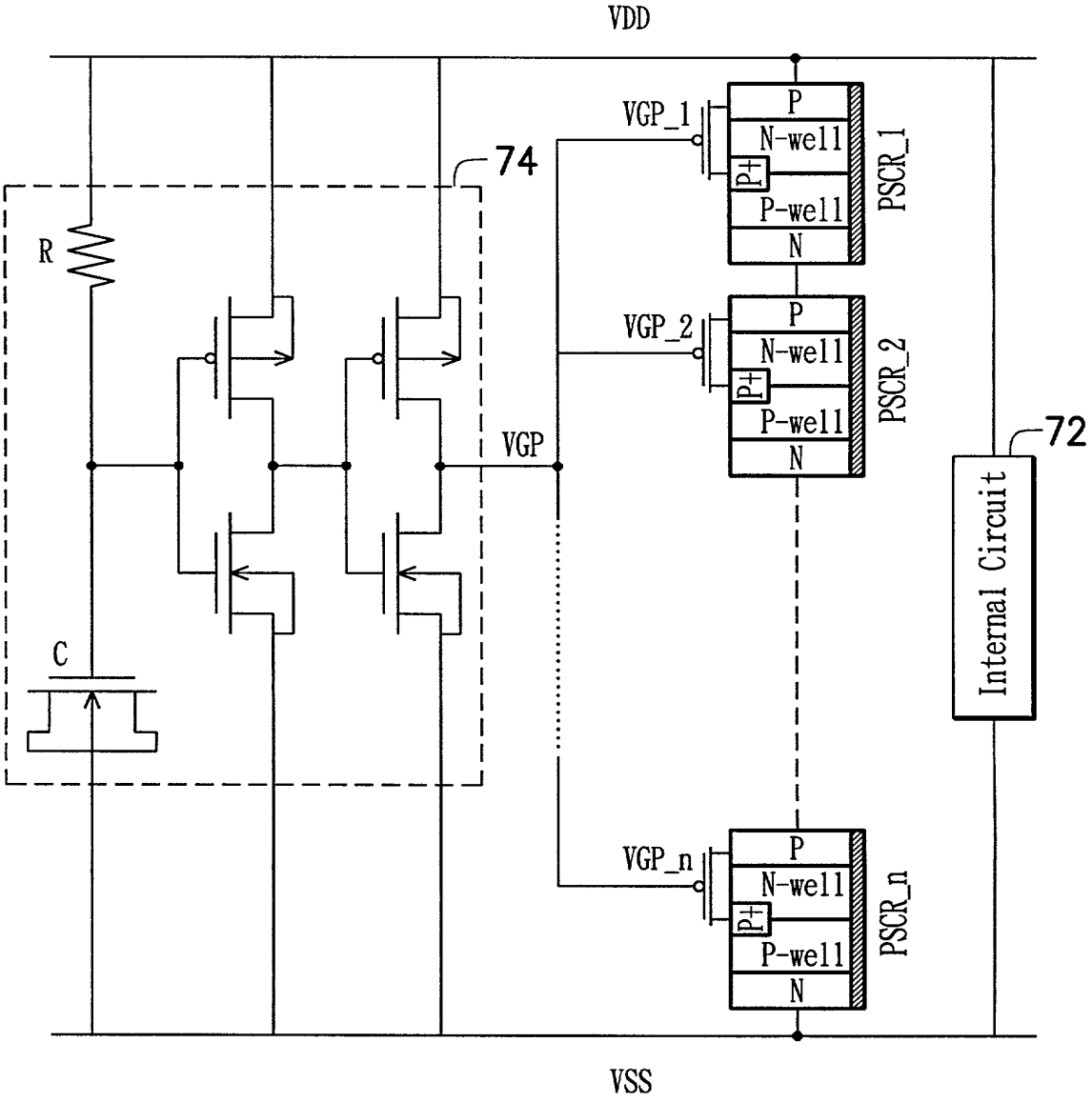
VDD
VGP_1
P
N-well
P+
P-well
N
PSCR_1
74
R
VGP_2
PSCR_2
VGP
72
Internal Circuit
C
VGP_n
PSCR_n
VSS

FIG. 10

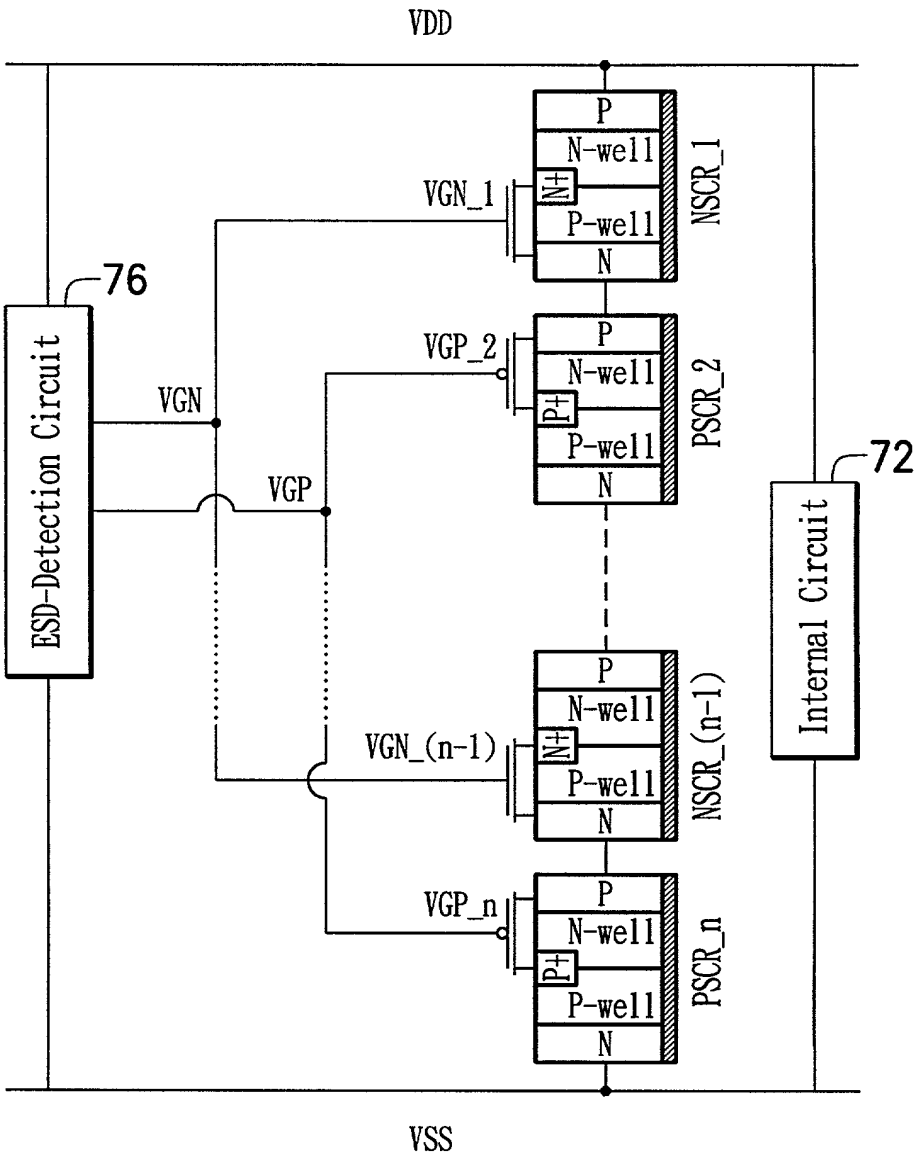
VDD
P
N-well
N+
P-well
N
NSCR_1
VGN_1
76
ESD-Detection Circuit
VGN
VGP_2
P+
PSCR_2
VGP
72
Internal Circuit
VGN_(n-1)
NSCR_(n-1)
VGP_n
PSCR_n
VSS

FIG. 11

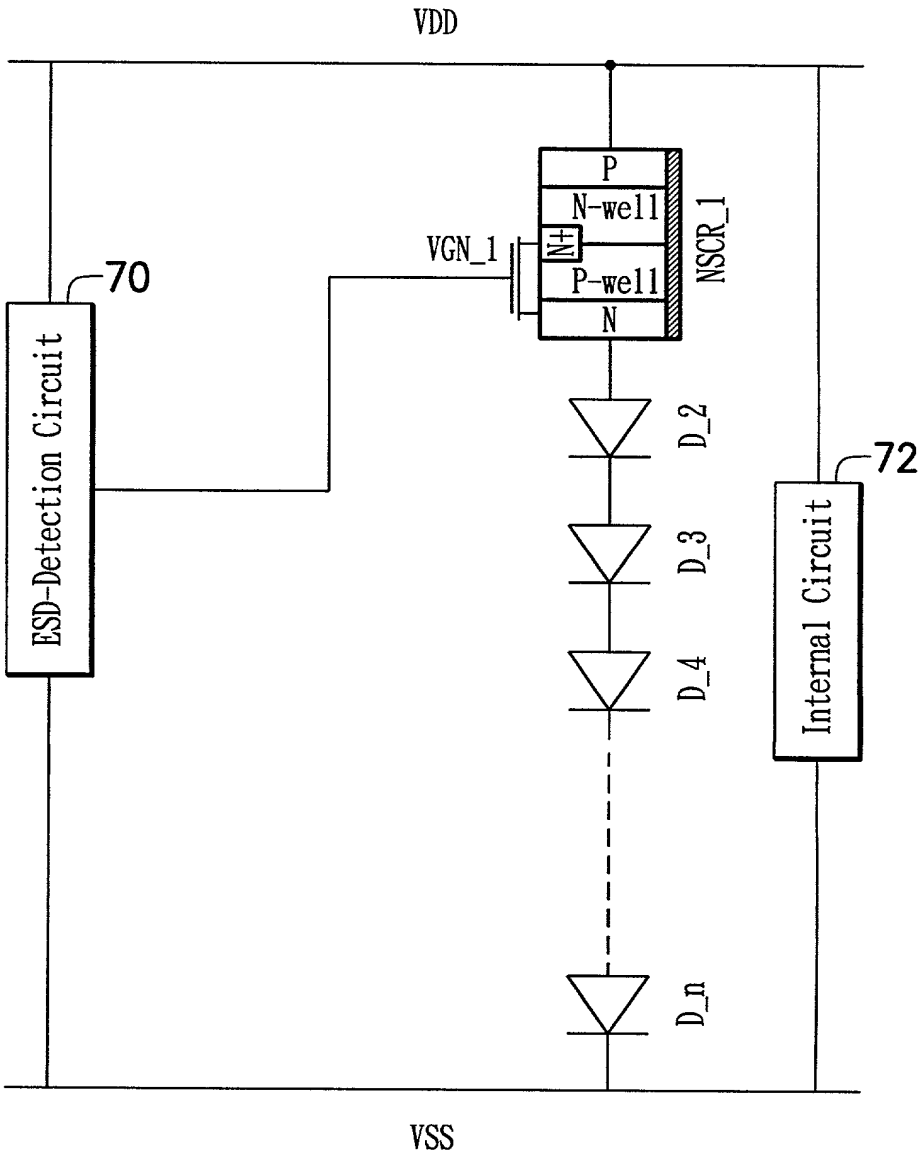
VDD
P
N-well
N+
P-well
N
NSCR_1
VGN_1
70
ESD-Detection Circuit
D_2
D_3
D_4
D_n
72
Internal Circuit
VSS

FIG. 12

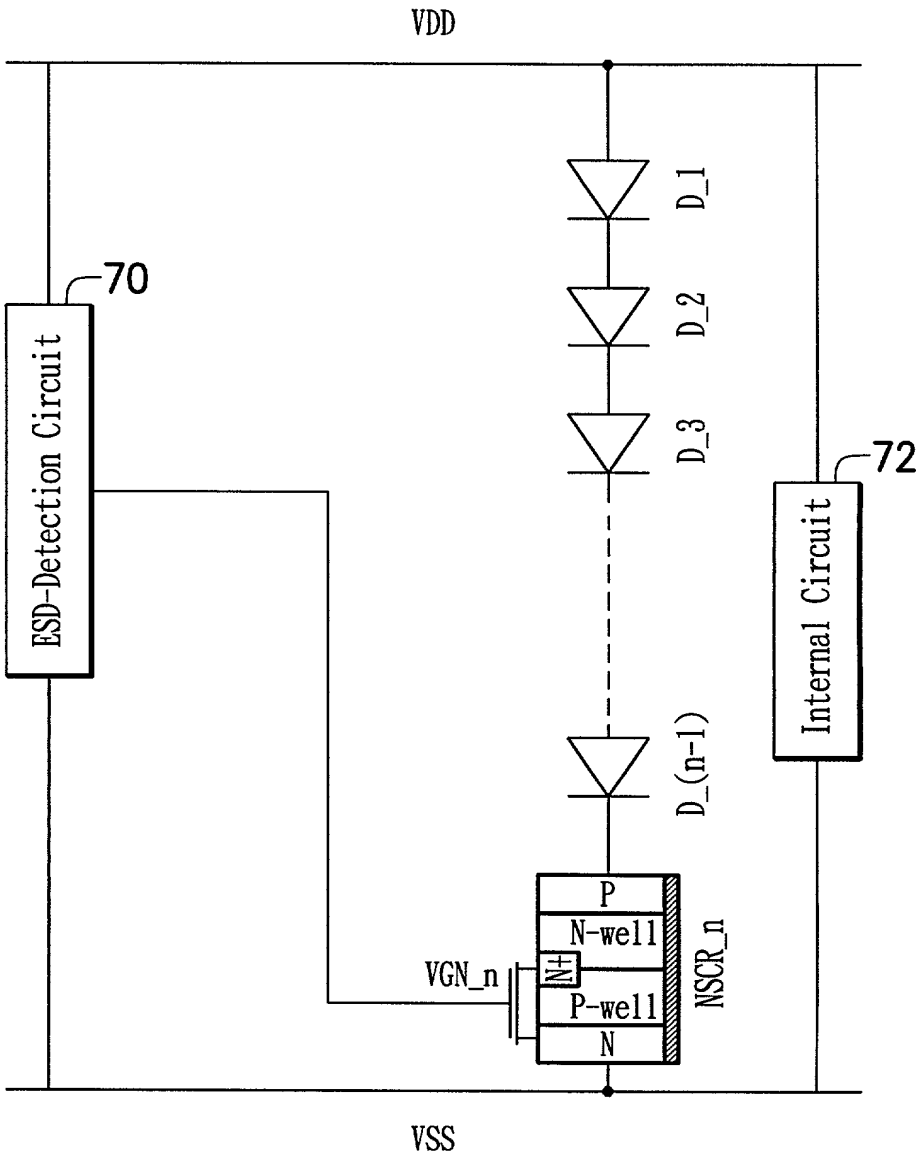
VDD
70
ESD-Detection Circuit
D_1
D_2
D_3
D_(n-1)
72
Internal Circuit
P
N-well
N+
VGN_n
P-well
N
NSCR_n
VSS

FIG. 13

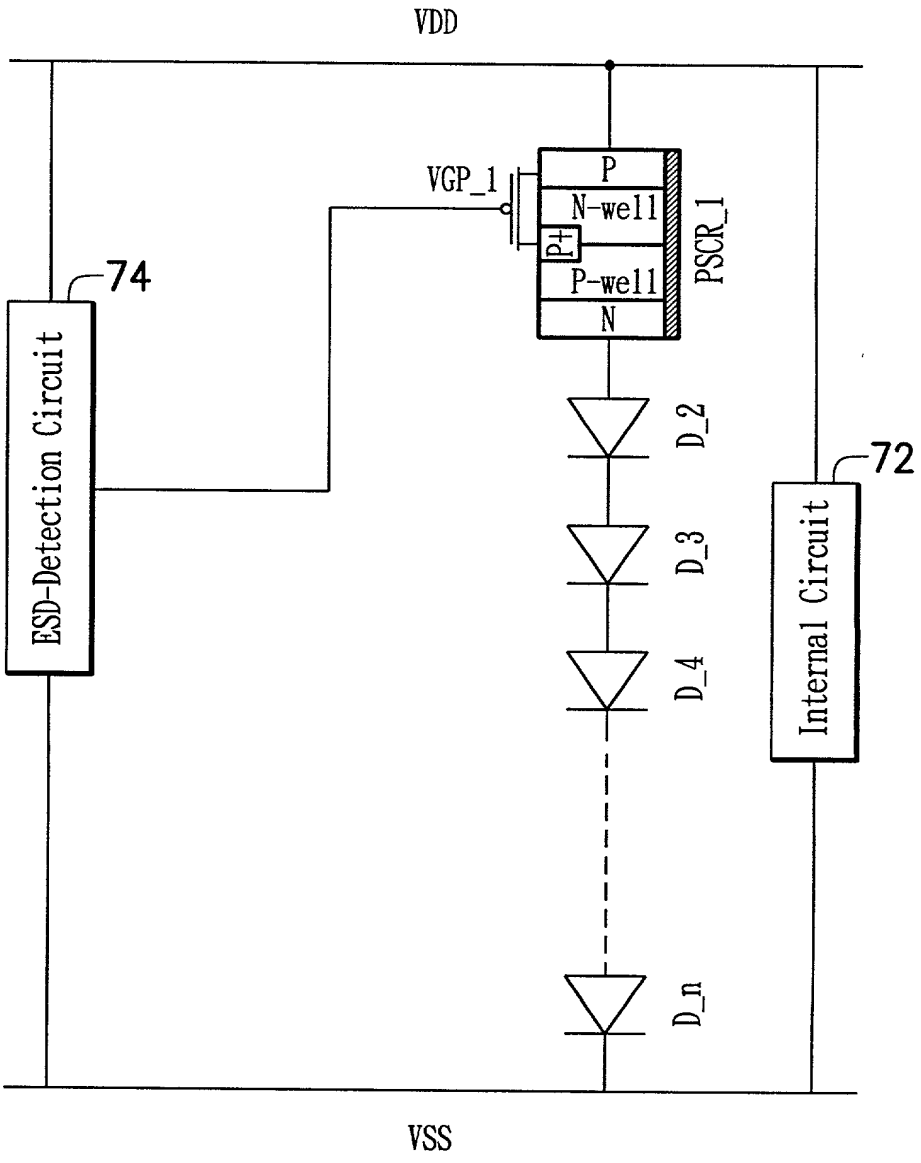
VDD
VGP_1
P
N-well
P+
P-well
N
PSCR_1
74
ESD-Detection Circuit
D_2
D_3
D_4
D_n
72
Internal Circuit
VSS

FIG. 14

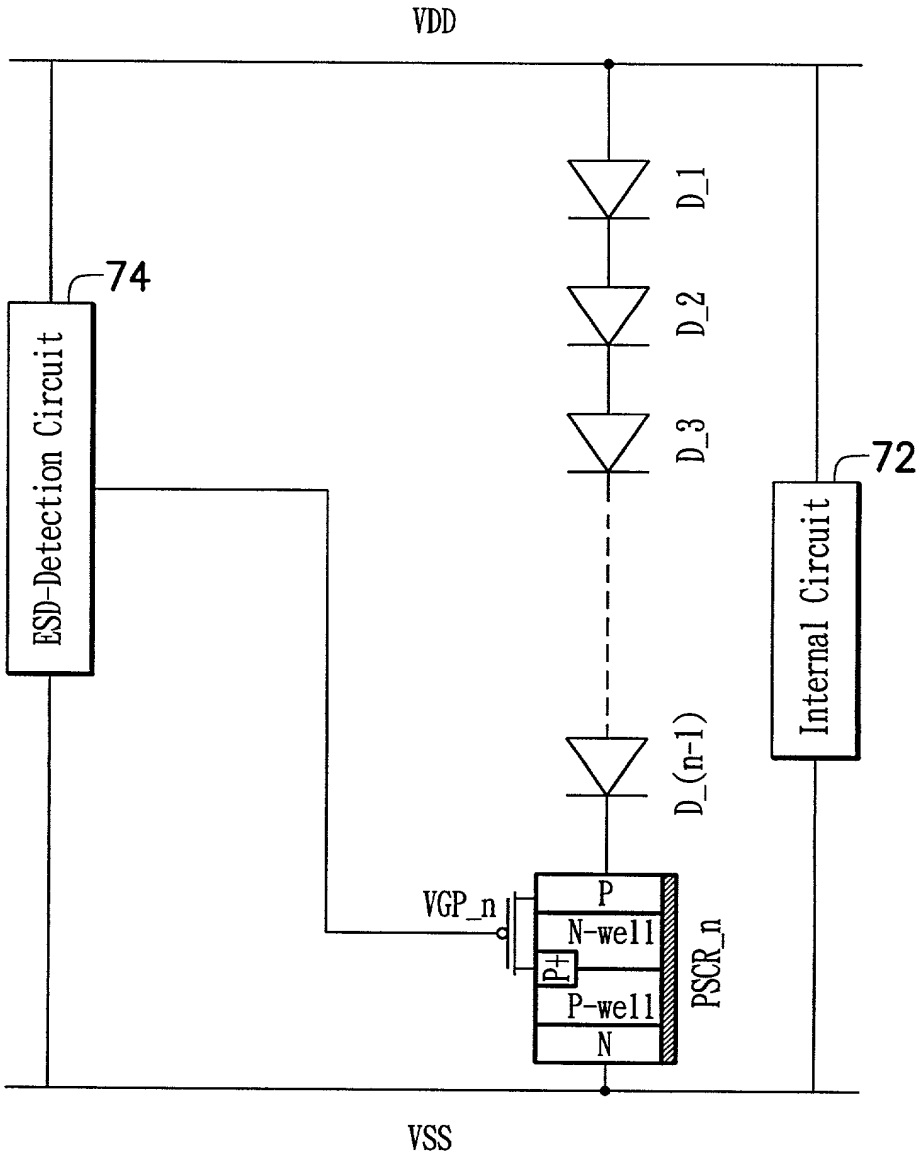
VDD
74
ESD-Detection Circuit
D_1
D_2
D_3
D_(n-1)
72
Internal Circuit
VGP_n
P
N-well
P+
P-well
N
PSCR_n
VSS

FIG. 15

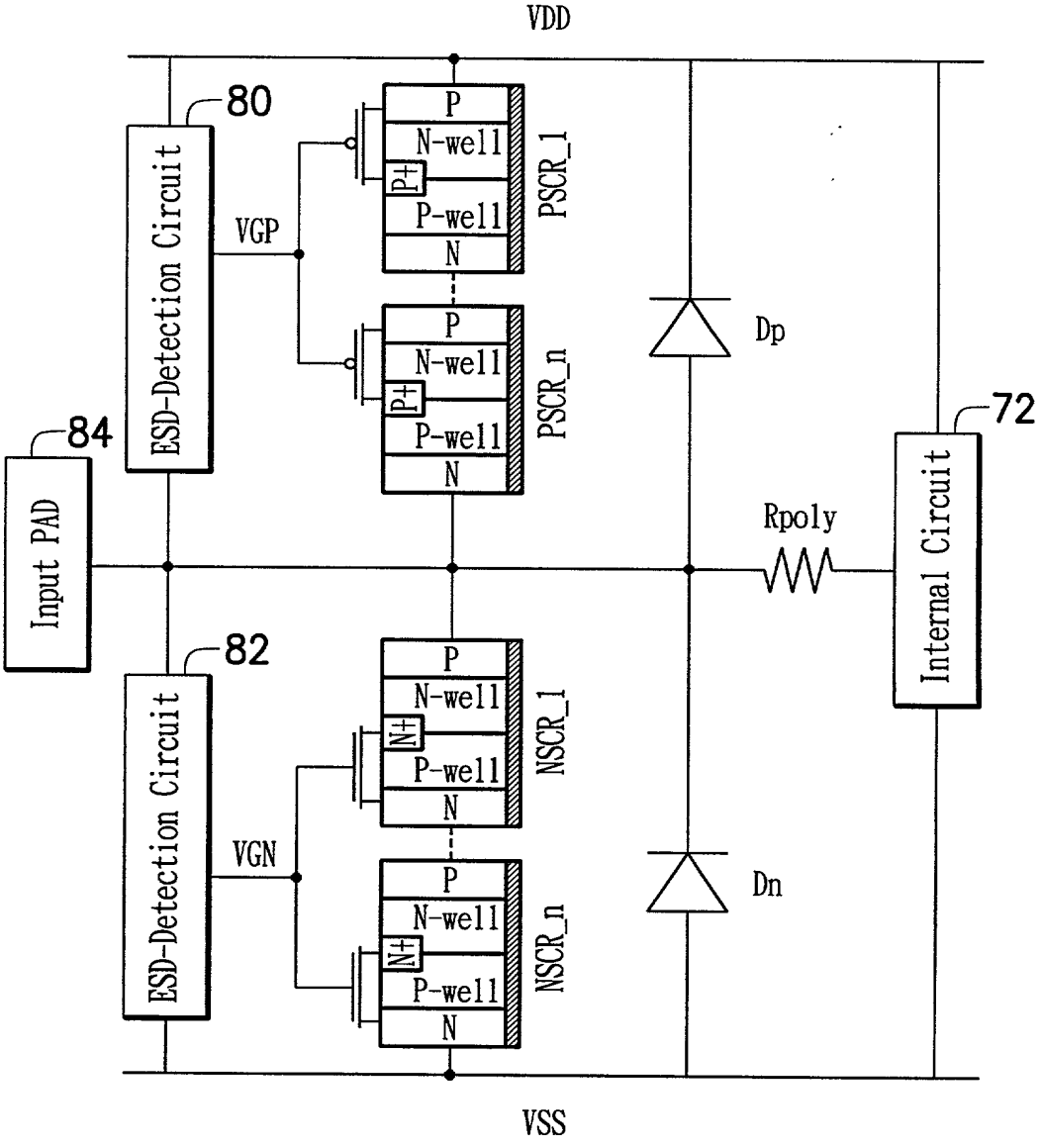
VDD
80
ESD-Detection Circuit
VGP
P
N-well
P+
P-well
N
PSCR_1
PSCR_n
Dp
84
Input PAD
Rpoly
72
Internal Circuit
82
ESD-Detection Circuit
VGN
N+
NSCR_1
NSCR_n
Dn
VSS

FIG. 16

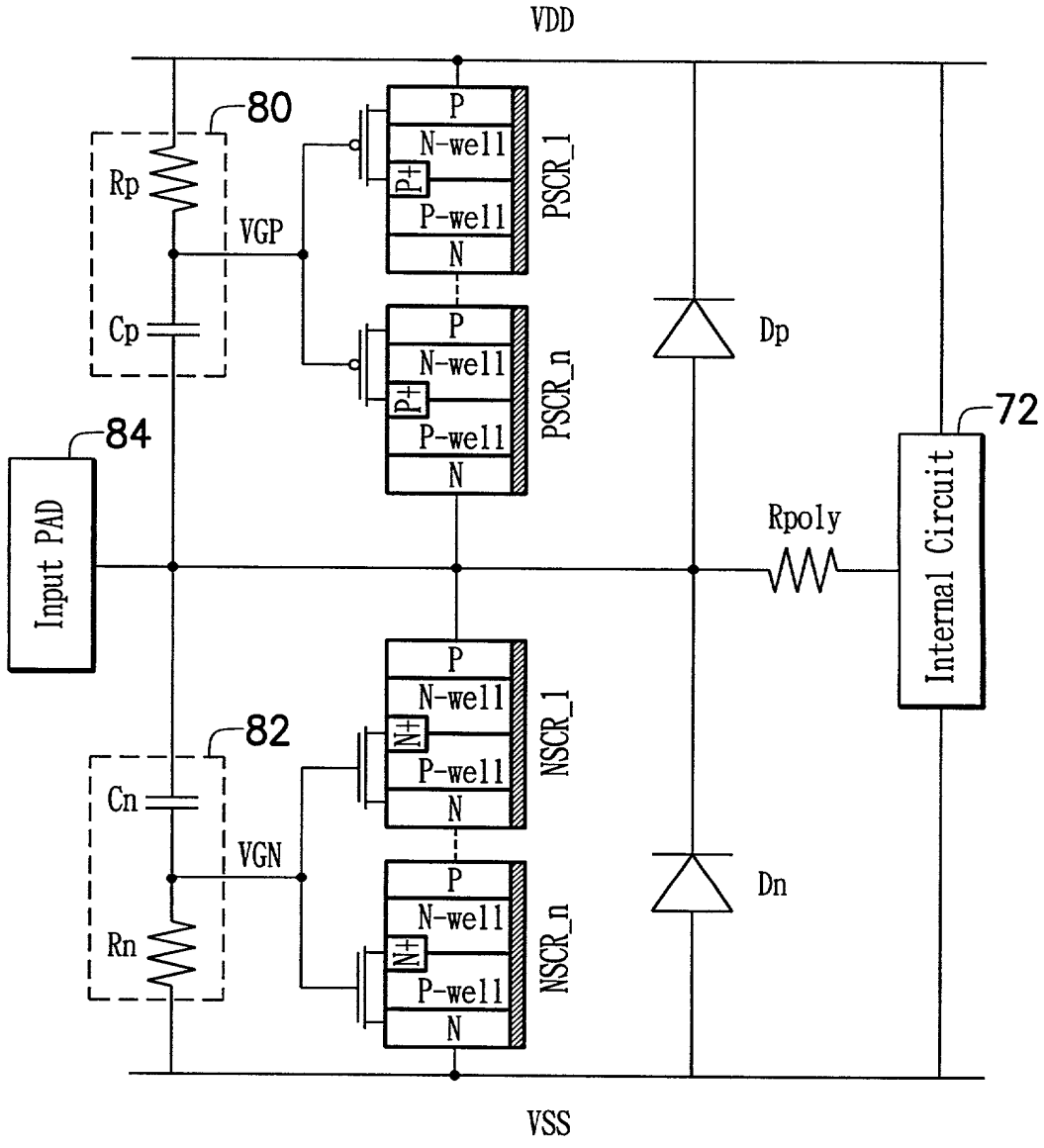
VDD
80
Rp
VGP
Cp
P
N-well
P+
P-well
N
PSCR_1
PSCR_n
Dp
72
84
Input PAD
Rpoly
Internal Circuit
82
Cn
VGN
Rn
N+
NSCR_1
NSCR_n
Dn
VSS

FIG. 17

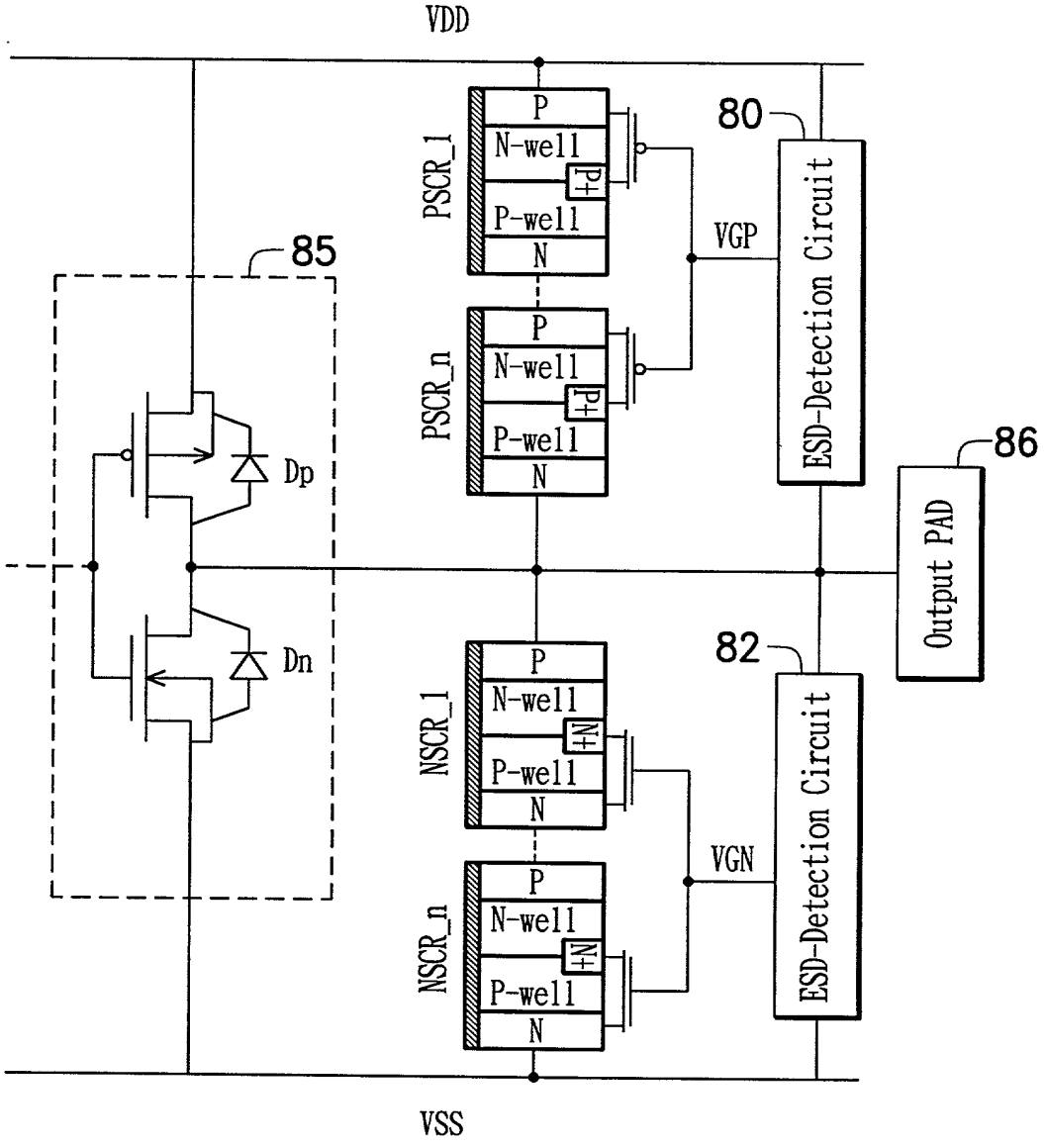
VDD
80
P
N-well
P+
P-well
N
PSCR_1
VGP
85
PSCR_n
ESD-Detection Circuit
86
Dp
Output PAD
Dn
82
N+
NSCR_1
VGN
NSCR_n
ESD-Detection Circuit
VSS

FIG. 18

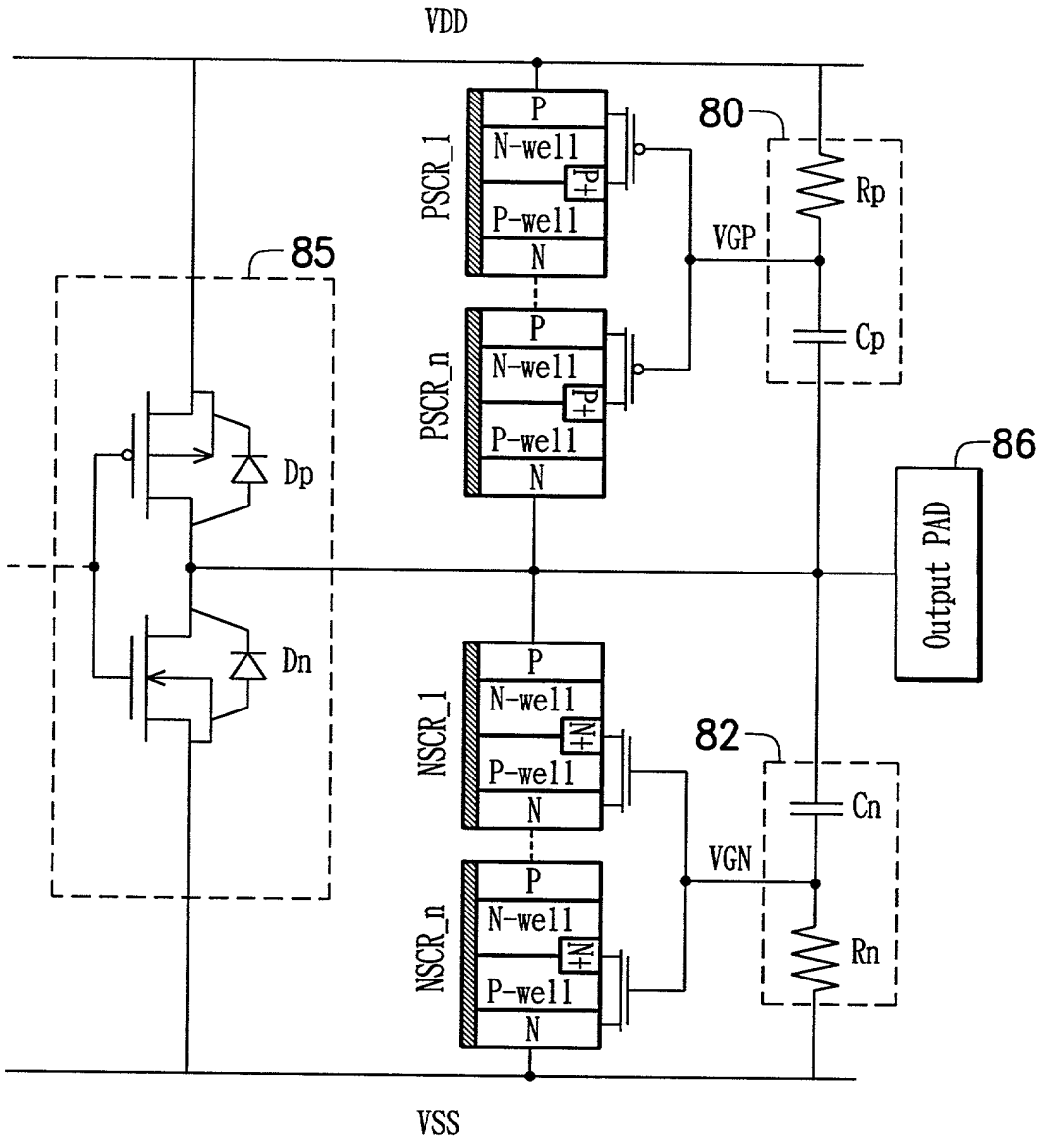
VDD
80
P
N-well
P+
P-well
N
PSCR_1
PSCR_n
VGP
Rp
Cp
85
Dp
Dn
86
Output PAD
N+
NSCR_1
NSCR_n
82
Cn
VGN
Rn
VSS

FIG. 19

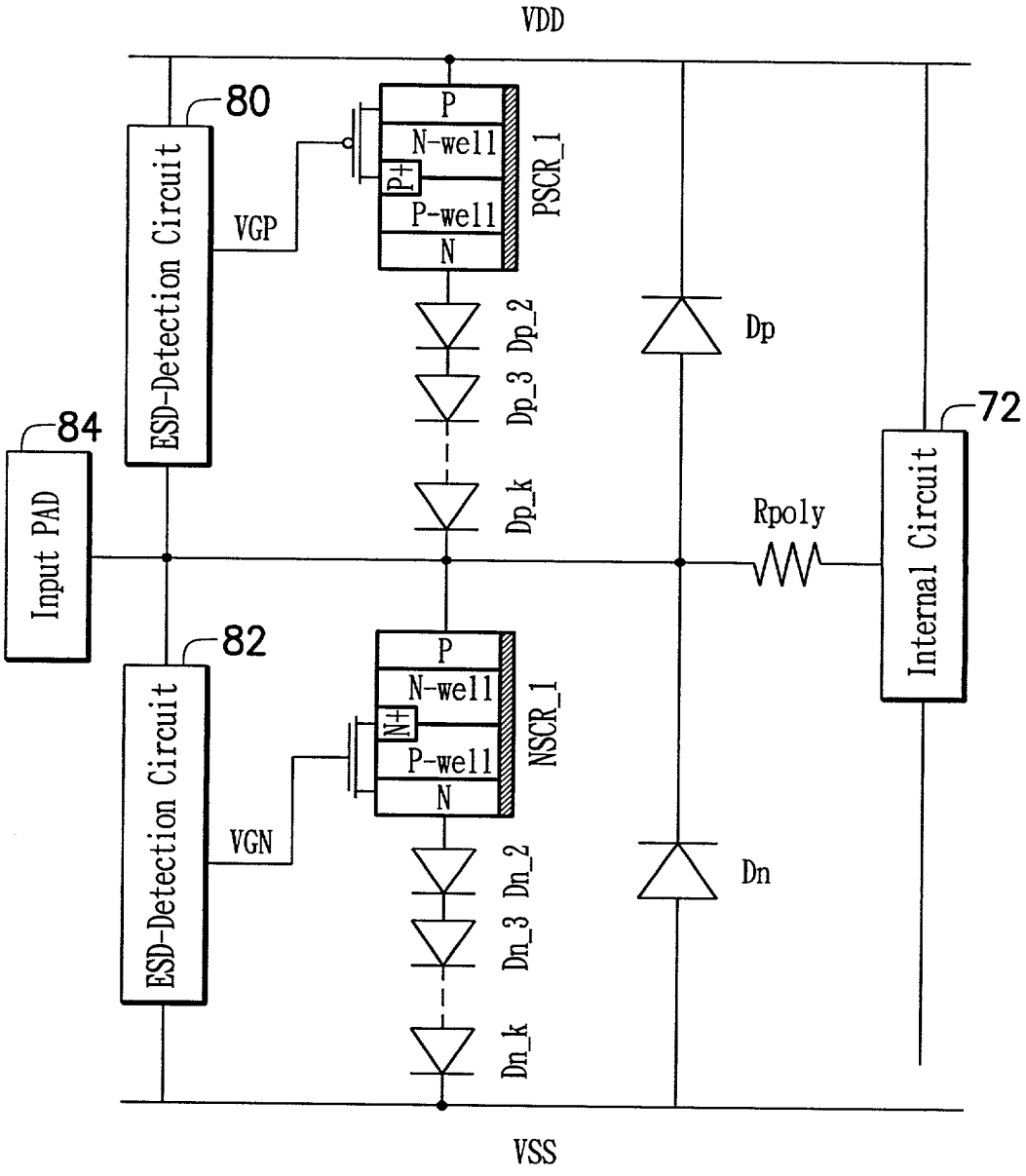
VDD
80
ESD-Detection Circuit
VGP
P
N-well
P+
P-well
N
PSCR_1
Dp_2
Dp_3
Dp_k
Dp
84
Input PAD
72
Internal Circuit
Rpoly
82
ESD-Detection Circuit
VGN
P
N-well
N+
P-well
N
NSCR_1
Dn_2
Dn_3
Dn_k
Dn
VSS

FIG. 20

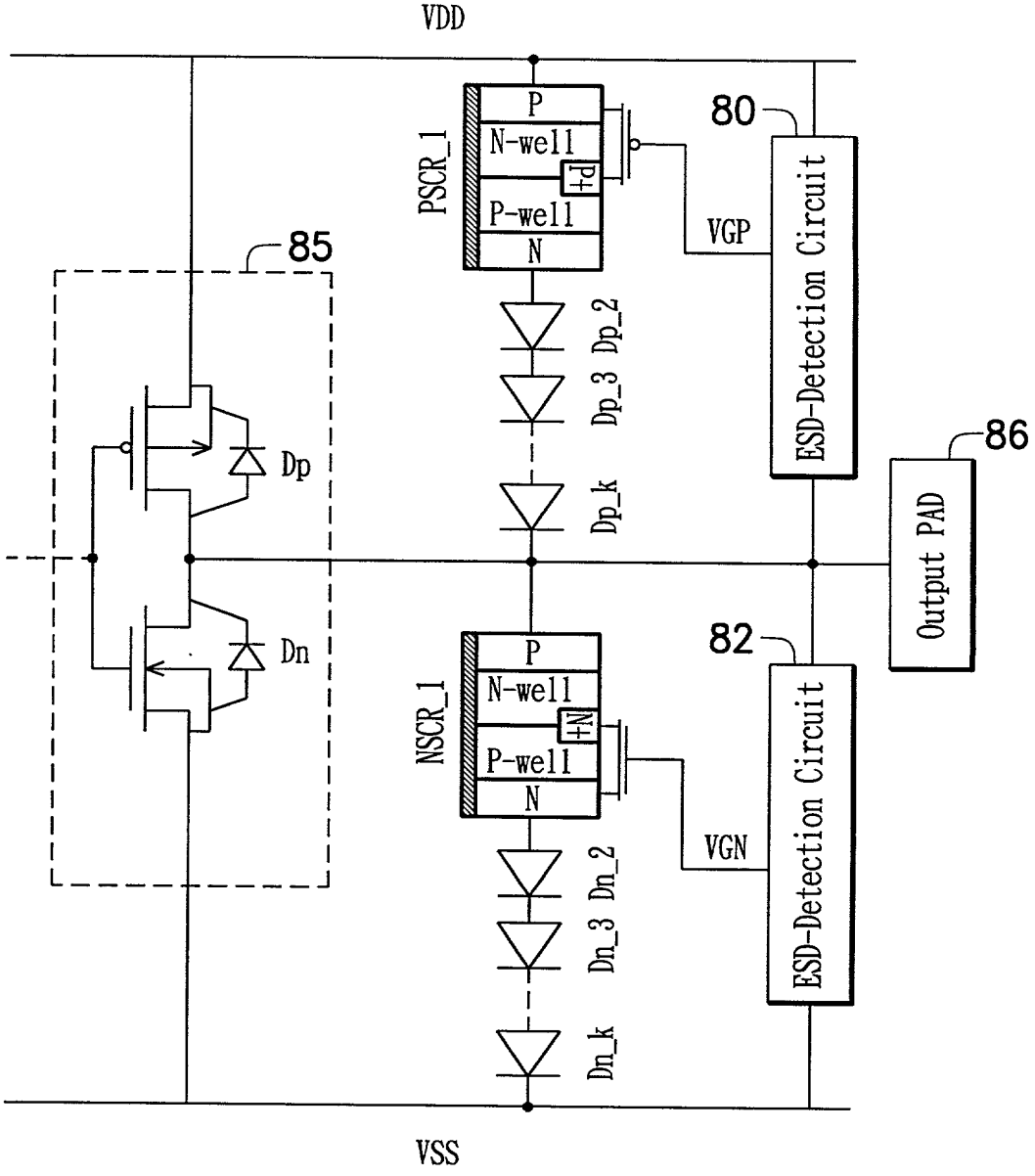
VDD
P
N-well
+d
P-well
N
PSCR_1
80
VGP
ESD-Detection Circuit
85
Dp
Dp_2
Dp_3
Dp_k
86
Output PAD
Dn
82
P
N-well
+N
P-well
N
NSCR_1
VGN
ESD-Detection Circuit
Dn_2
Dn_3
Dn_k
VSS

FIG. 21

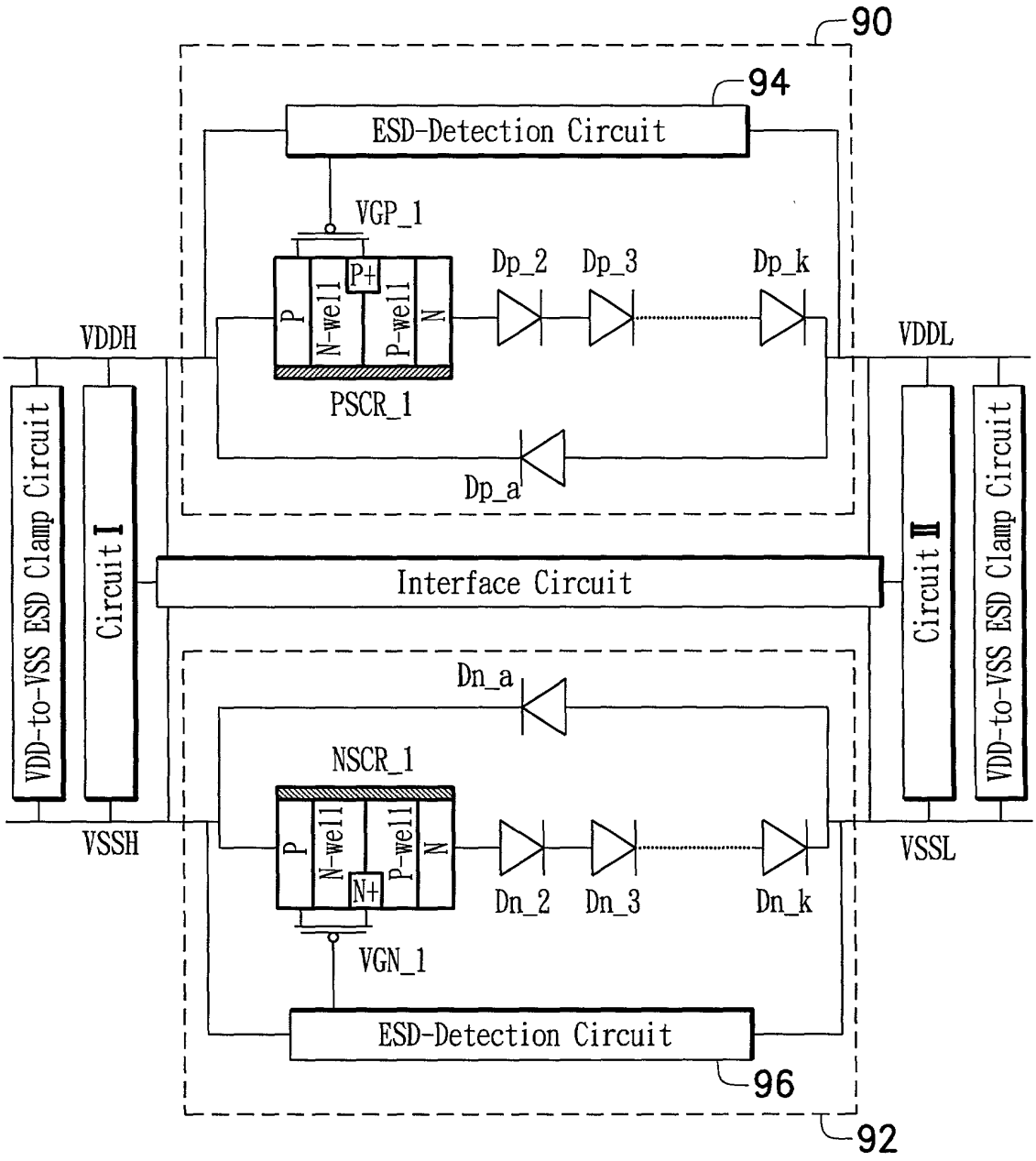
90
94
ESD-Detection Circuit
VGP_1
P+
P
N-well
P-well
N
Dp_2
Dp_3
Dp_k
VDDH
VDDL
PSCR_1
Dp_a
VDD-to-VSS ESD Clamp Circuit
Circuit I
Interface Circuit
Circuit II
VDD-to-VSS ESD Clamp Circuit
Dn_a
NSCR_1
N+
Dn_2
Dn_3
Dn_k
VSSH
VSSL
VGN_1
ESD-Detection Circuit
96
92

FIG. 22

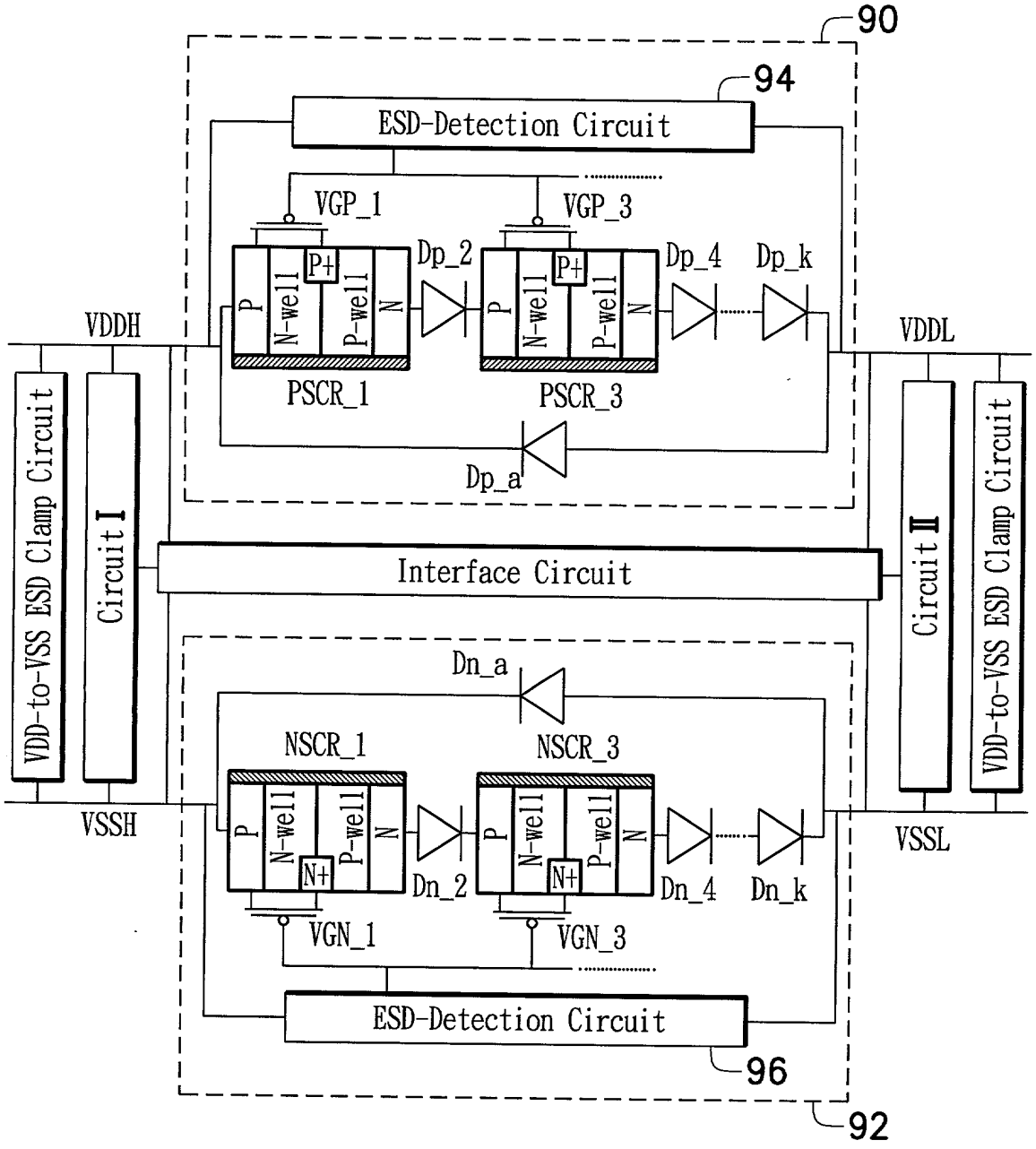
90
94
ESD-Detection Circuit
VGP_1
VGP_3
Dp_2
Dp_4
Dp_k
P+
P
N-well
P-well
N
PSCR_1
PSCR_3
Dp_a
VDDH
VDDL
VDD-to-VSS ESD Clamp Circuit
Circuit I
Interface Circuit
Circuit II
VDD-to-VSS ESD Clamp Circuit
Dn_a
NSCR_1
NSCR_3
N+
Dn_2
Dn_4
Dn_k
VGN_1
VGN_3
VSSH
VSSL
ESD-Detection Circuit
96
92

FIG. 23